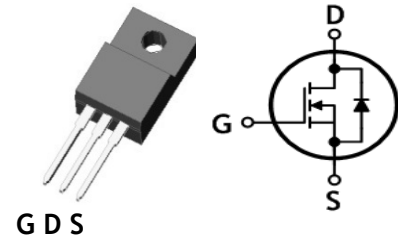


SWITCHING REGULATOR APPLICATION

Features

- Drain-Source breakdown voltage: $V_{DSS}=800V$
- Low gate charge: $Q_g=58nC$ (Typ.)
- Low drain-source On resistance: $R_{DS(on)}=1.1\Omega$ (Max.)
- RoHS compliant device
- 100% avalanche tested

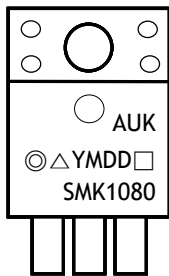


TO-220F-3L

Ordering Information

Part Number	Marking	Package
SMK1080FD	SMK1080	TO-220F-3L

Marking Information



- AUK = Manufacture Logo
 ◎ = Management Code
 △ = Machine Code
 YMDD = Date Code Marking
 -. YMDD = Date Code (year, week, daily)
 □ = Factory Management Code
 SMK1080 = Specific Device Code

Absolute maximum ratings ($T_C=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	800	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current (DC) *	I_D	$T_C=25^\circ C$	10	A
		$T_C=100^\circ C$	6.32	A
Drain current (Pulsed) *	I_{DM}	40	A	
Single pulsed avalanche energy (Note 2)	E_{AS}	800	mJ	
Repetitive avalanche current (Note 1)	I_{AR}	10	A	
Repetitive avalanche energy (Note 1)	E_{AR}	4.8	mJ	
Power dissipation	P_D	48	W	
Junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55-150	$^\circ C$	

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.6	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	800	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	3	-	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=800\text{V}$, $V_{GS}=0\text{V}$	-	-	1	uA
		$V_{DS}=640\text{V}$, $T_C=125^\circ\text{C}$	-	-	100	uA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=5\text{A}$	-	0.93	1.1	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=40\text{V}$, $I_D=5\text{A}$	-	5.8	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	2630	-	pF
Output capacitance	C_{oss}		-	192	-	
Reverse transfer capacitance	C_{rss}		-	18	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=400\text{V}$, $I_D=10\text{A}$, $R_G=25\Omega$	-	50	-	ns
Rise time (Note 3,4)	t_r		-	130	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	90	-	
Fall time (Note 3,4)	t_f		-	80	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=640\text{V}$, $V_{GS}=10\text{V}$, $I_D=10\text{A}$	-	58	-	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	21	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	18	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	10	A
Source current (Pulsed)	I_{SM}		-	-	40	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=10\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=10\text{A}$, $V_{GS}=0\text{V}$ $di_F/dt=100\text{A}/\mu\text{s}$	-	650	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	10.9	-	uC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=15\text{mH}$, $I_{AS}=10\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristics Curves

Fig. 1 $I_D - V_{DS}$

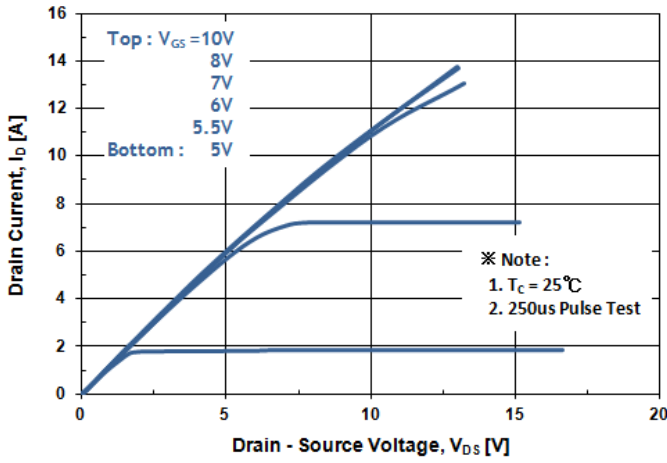


Fig. 2 $I_D - V_{GS}$

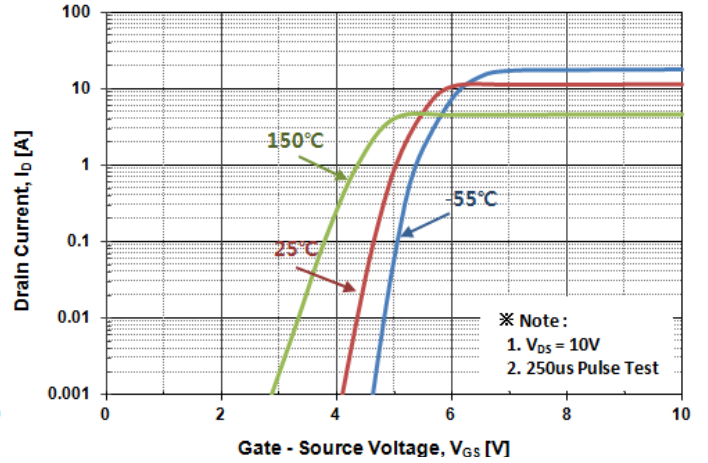


Fig. 3 $R_{DS(ON)} - I_D$

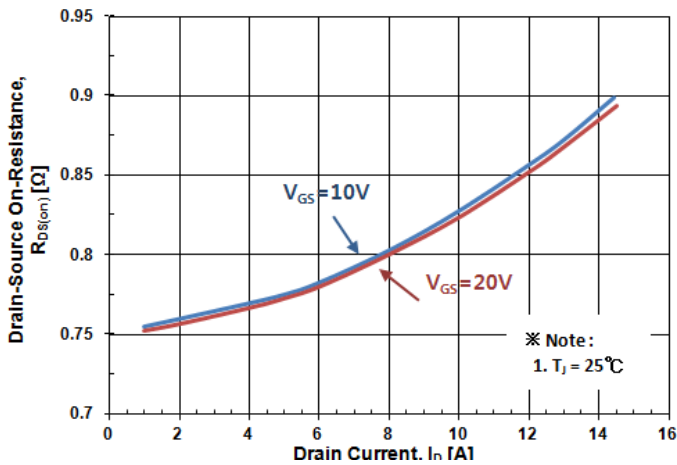


Fig. 4 $I_S - V_{SD}$

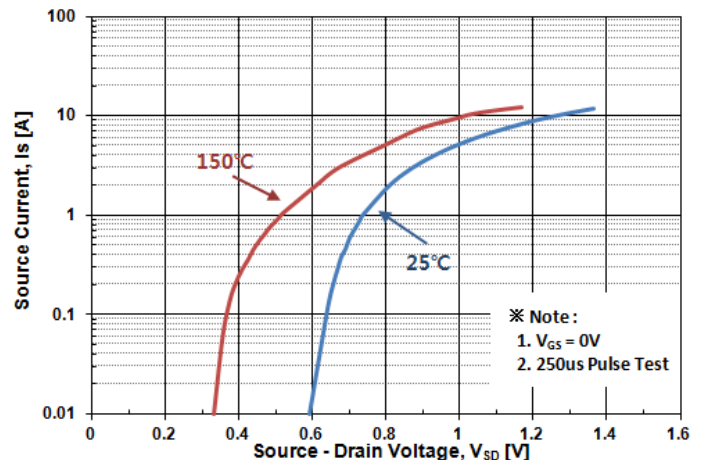


Fig. 5 Capacitance - V_{DS}

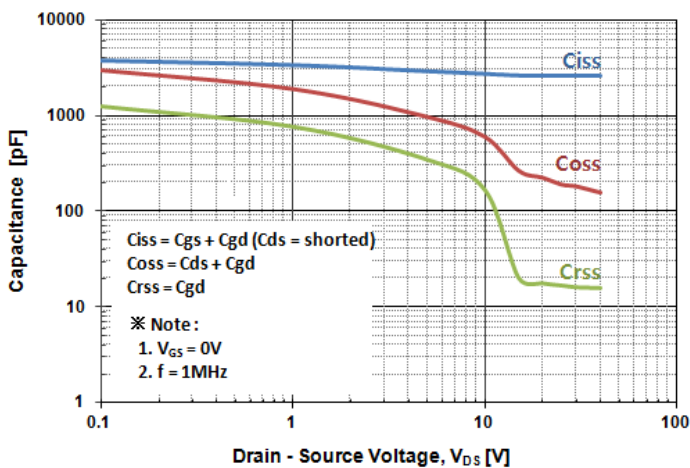
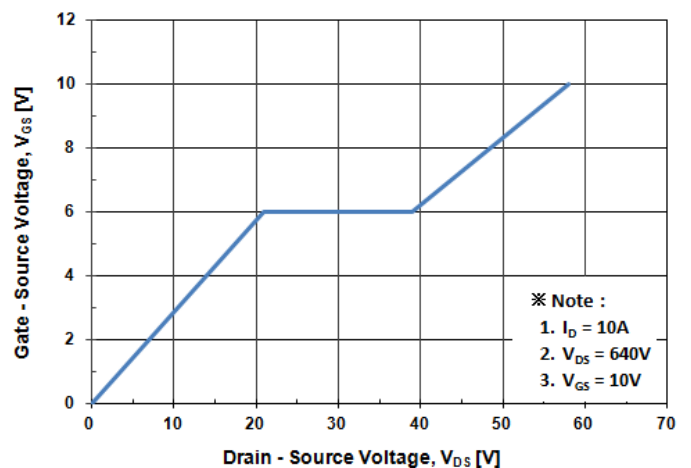


Fig. 6 $V_{GS} - Q_G$



Electrical Characteristics Curves

Fig. 7 $V_{ncc} - T_J$

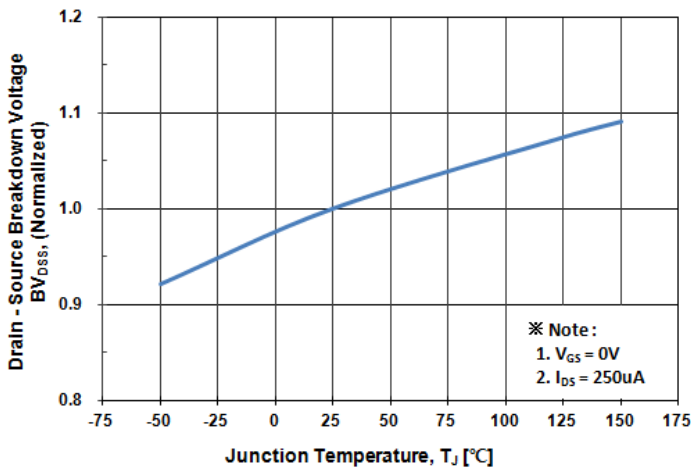


Fig. 8 $R_{DS(on)} - T_J$

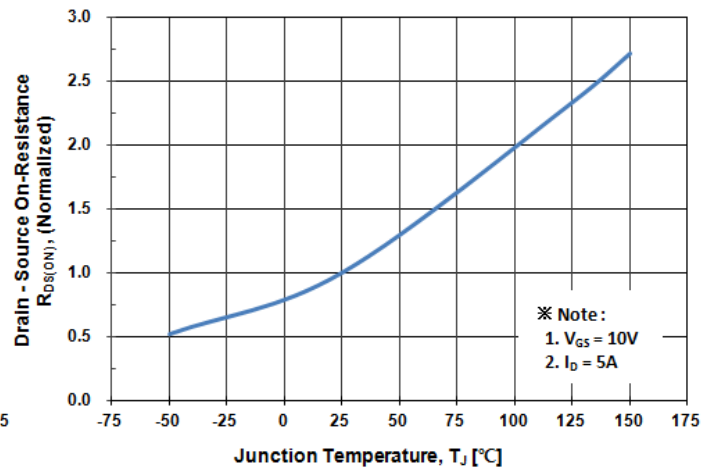


Fig. 9 $I_D - T_C$

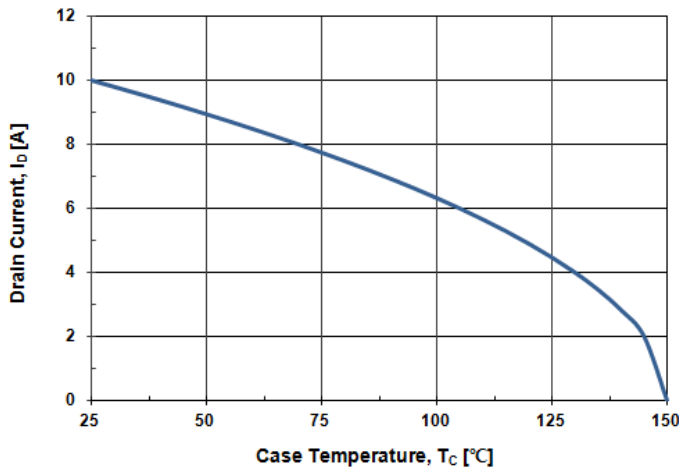


Fig. 10 Safe Operating Area

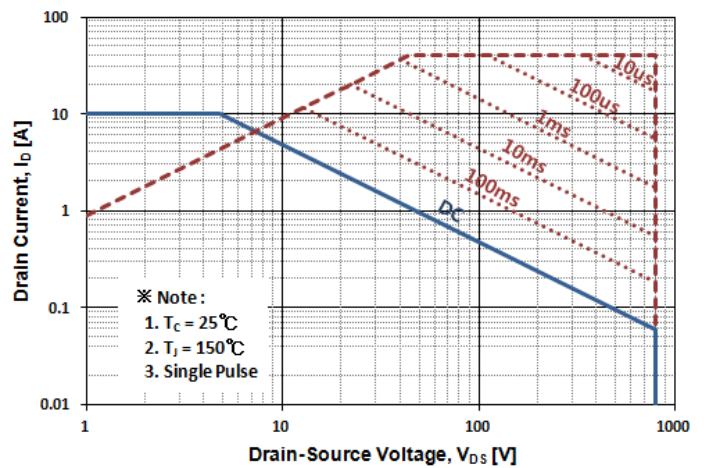


Fig. 11 Transient Thermal Impedance

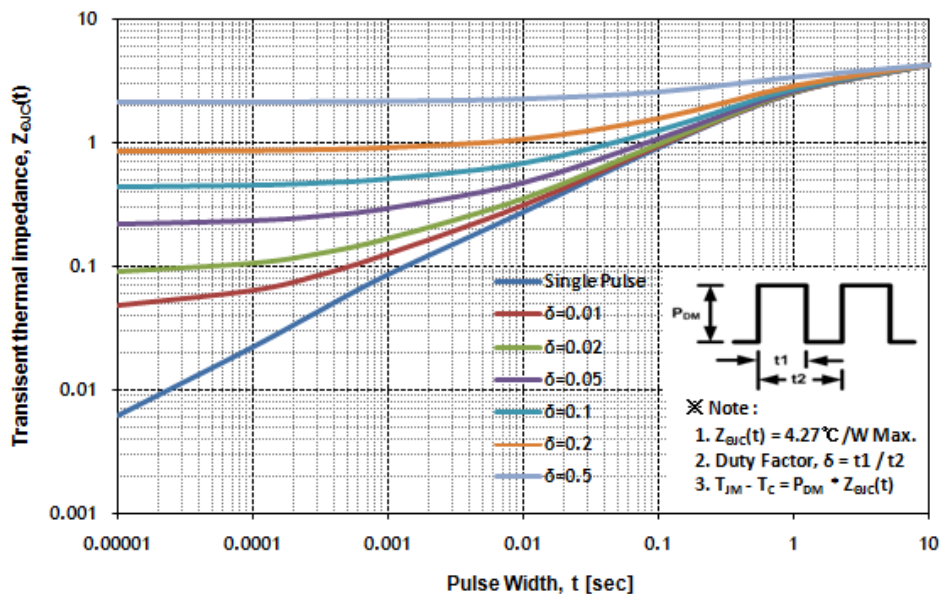


Fig. 12 Gate Charge Test Circuit & Waveform

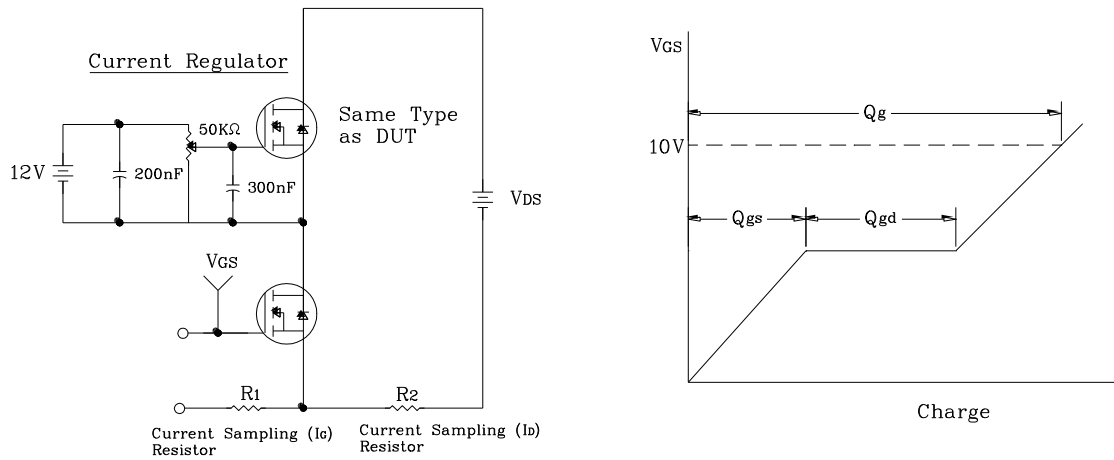


Fig. 13 Resistive Switching Test Circuit & Waveform

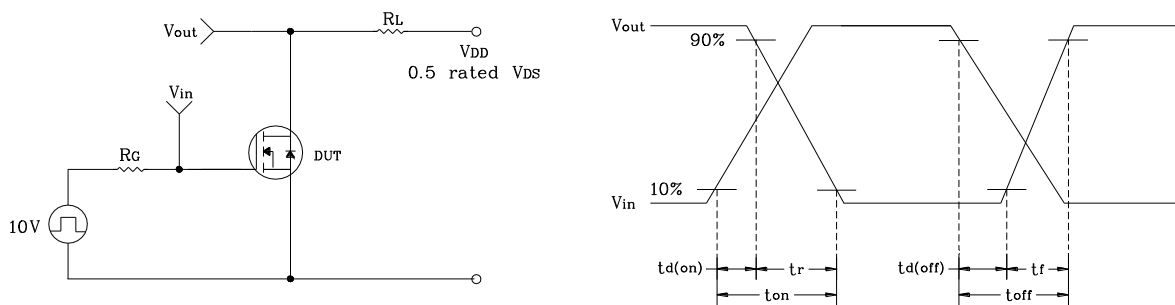


Fig. 14 E_{AS} Test Circuit & Waveform

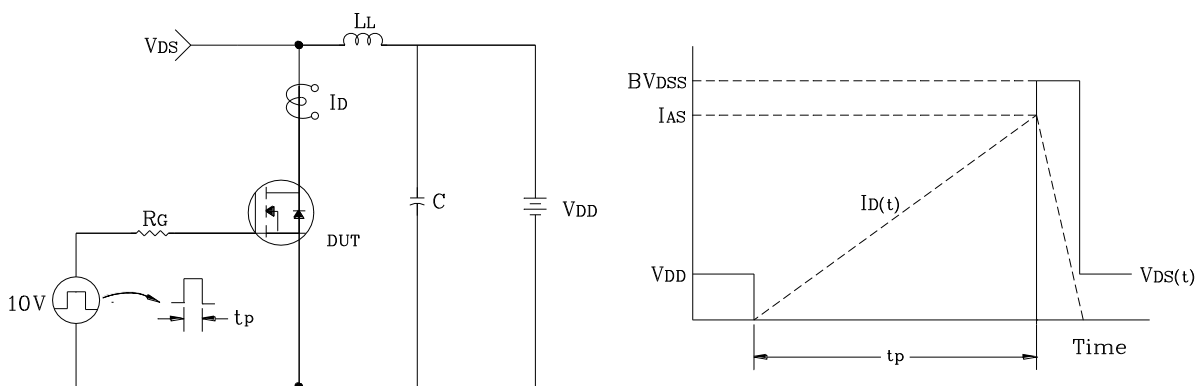
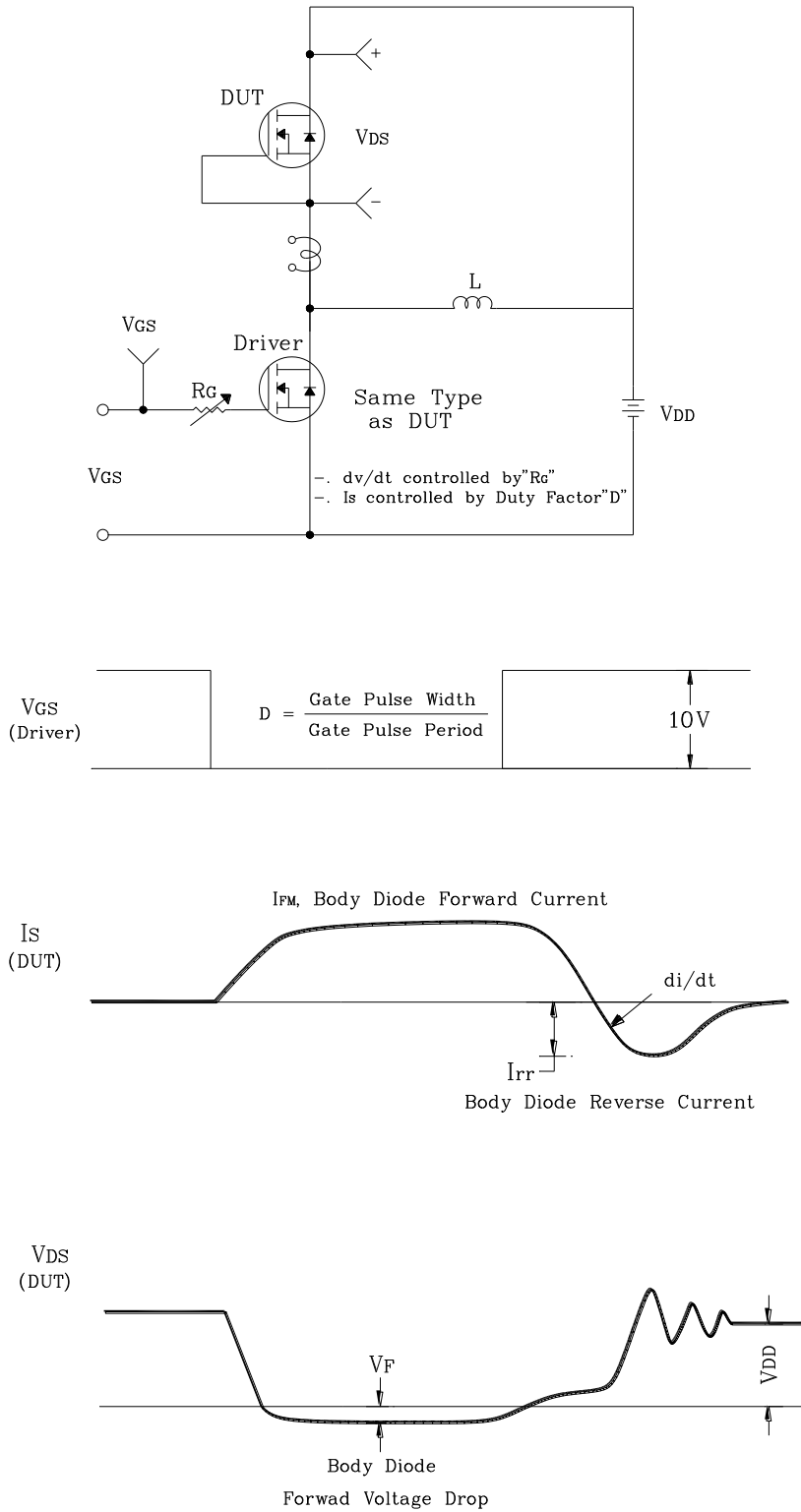
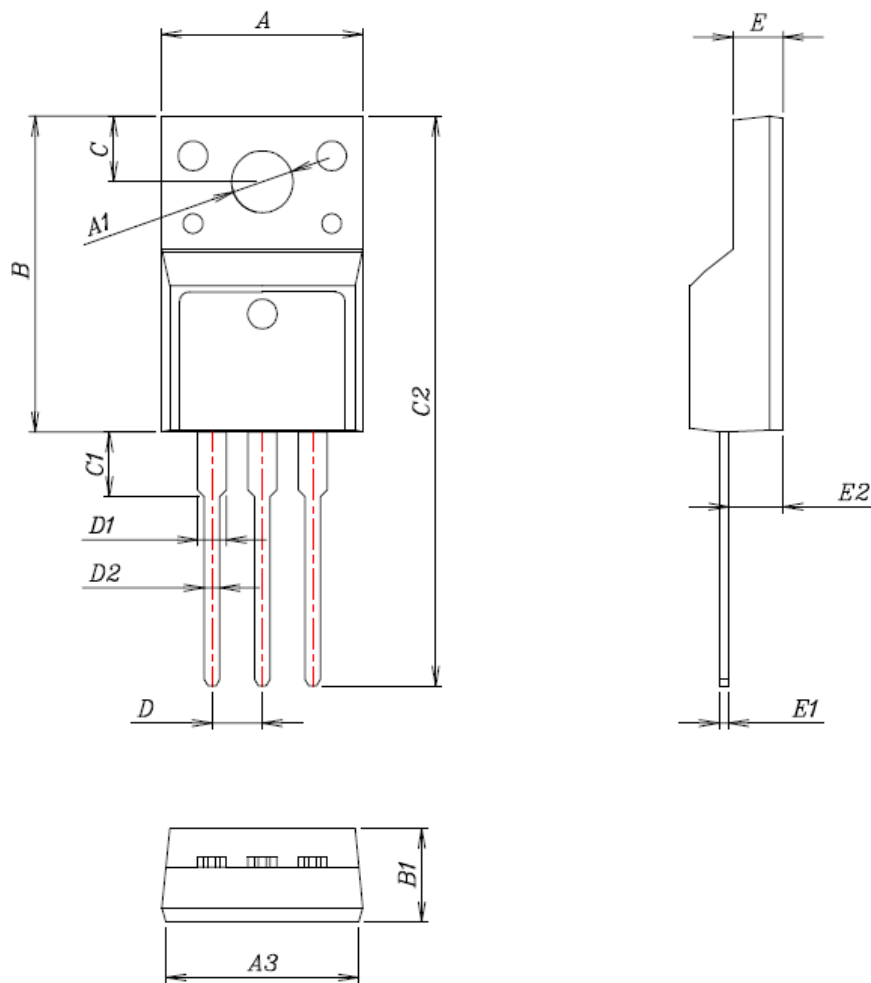


Fig. 15 Diode Reverse Recovery Time Test Circuit & Waveform



Package Outline Dimensions



SYMBOL	MILLIMETERS
A	10.16±0.30
A1	3.12±0.20
B	15.90±0.50
B1	4.70±0.30
C	3.30±0.25
C1	3.25±0.30
C2	28.70±0.50
D	Typical 2.54
D1	1.47(MAX)
D2	0.80±0.20
E	2.55±0.25
E1	0.50±0.20
E2	2.75±0.30

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